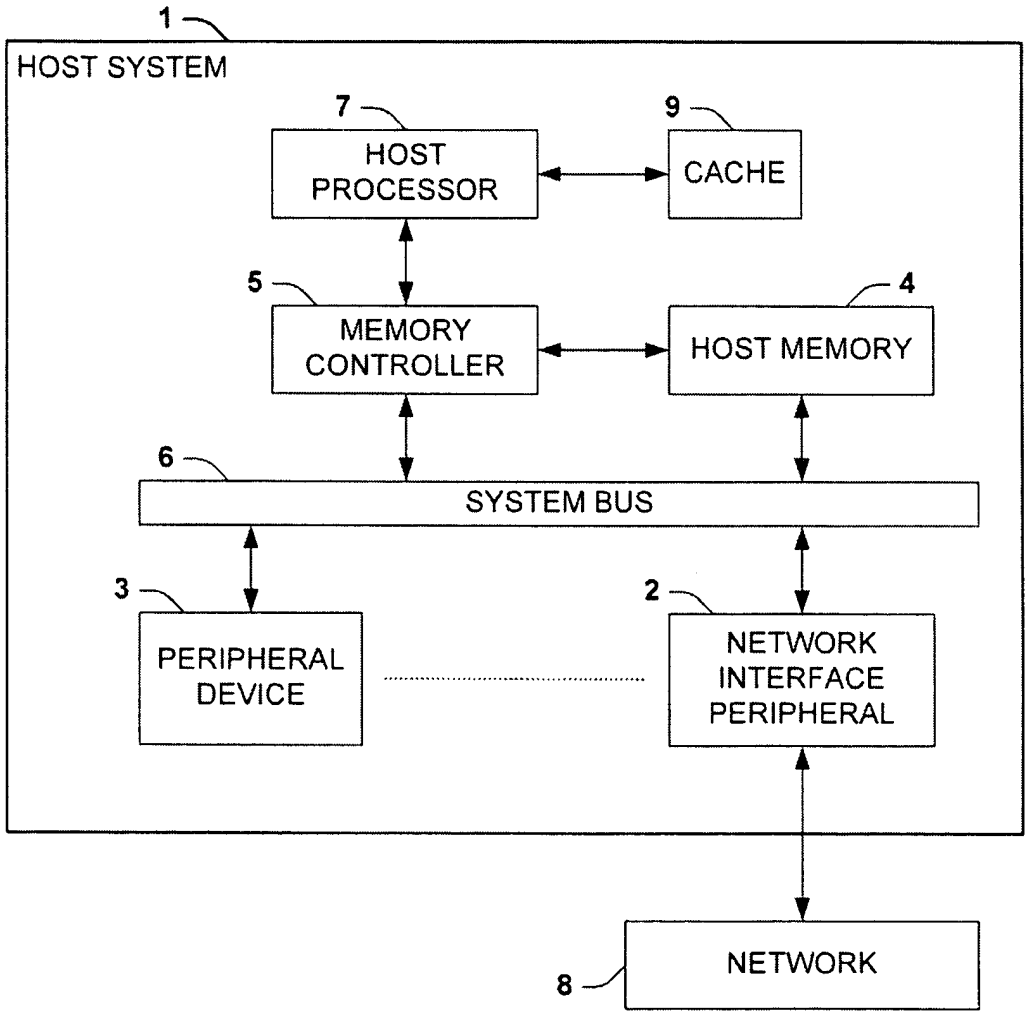
1
HOST SYSTEM
7
HOST PROCESSOR
9
CACHE
5
MEMORY CONTROLLER
4
HOST MEMORY
6
SYSTEM BUS
3
PERIPHERAL DEVICE
2
NETWORK INTERFACE PERIPHERAL
8
NETWORK

Fig. 1A

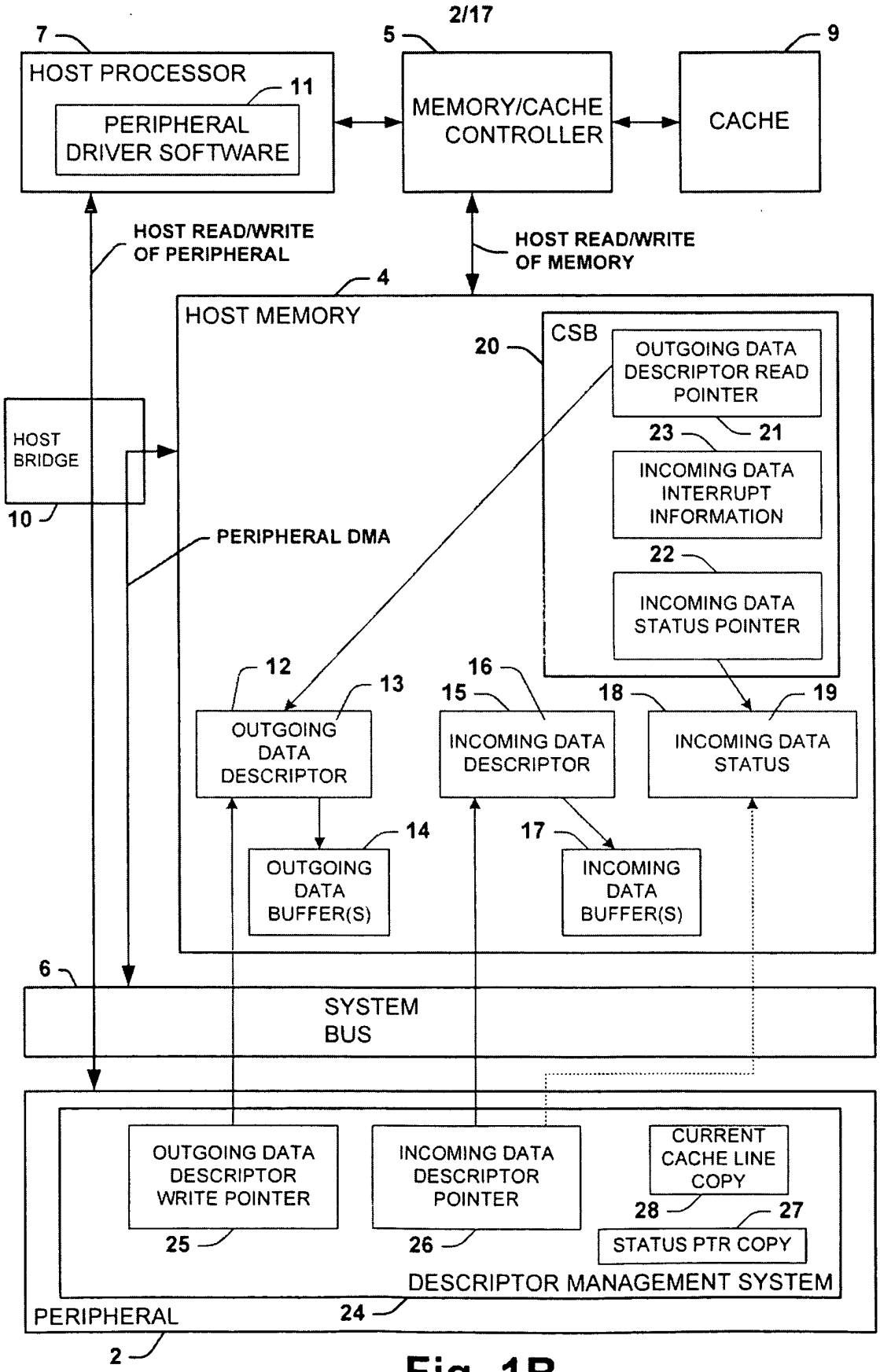
7
HOST PROCESSOR
11
PERIPHERAL DRIVER SOFTWARE
5
MEMORY/CACHE CONTROLLER
9
CACHE
HOST READ/WRITE OF PERIPHERAL
HOST READ/WRITE OF MEMORY
4
HOST MEMORY
CSB
20
OUTGOING DATA DESCRIPTOR READ POINTER
23
21
INCOMING DATA INTERRUPT INFORMATION
22
INCOMING DATA STATUS POINTER
HOST BRIDGE
10
PERIPHERAL DMA
12
13
OUTGOING DATA DESCRIPTOR
16
15
INCOMING DATA DESCRIPTOR
18
19
INCOMING DATA STATUS
14
OUTGOING DATA BUFFER(S)
17
INCOMING DATA BUFFER(S)
6
SYSTEM BUS
OUTGOING DATA DESCRIPTOR WRITE POINTER
25
INCOMING DATA DESCRIPTOR POINTER
26
CURRENT CACHE LINE COPY
28
27
STATUS PTR COPY
DESCRIPTOR MANAGEMENT SYSTEM
24
PERIPHERAL
2

Fig. 1B

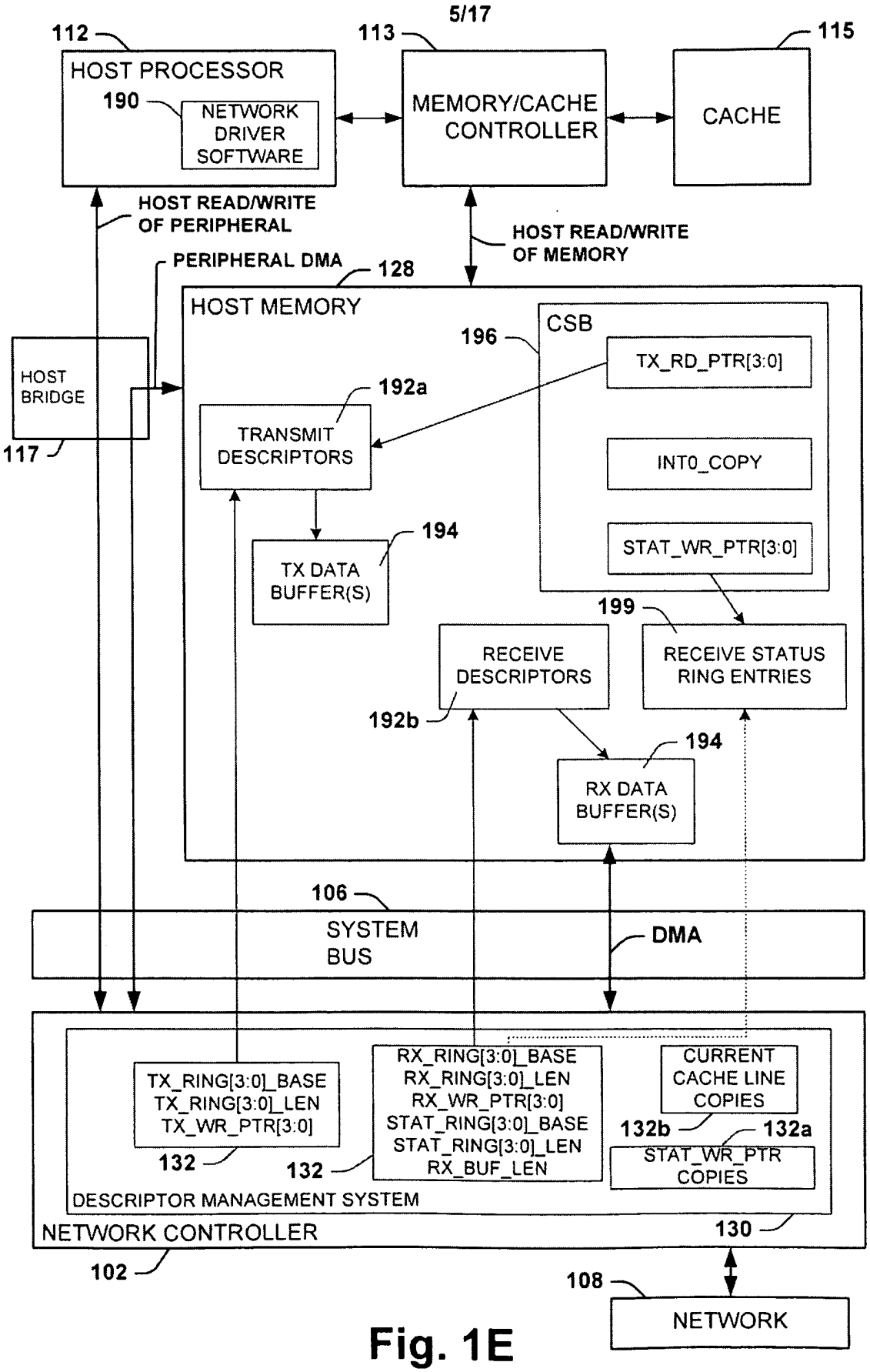
112
HOST PROCESSOR
190
NETWORK DRIVER SOFTWARE
113
MEMORY/CACHE CONTROLLER
115
CACHE
HOST READ/WRITE OF PERIPHERAL
HOST READ/WRITE OF MEMORY
PERIPHERAL DMA
128
HOST MEMORY
CSB
196
TX_RD_PTR[3:0]
HOST BRIDGE
117
192a
TRANSMIT DESCRIPTORS
INT0_COPY
194
TX DATA BUFFER(S)
STAT_WR_PTR[3:0]
199
RECEIVE DESCRIPTORS
RECEIVE STATUS RING ENTRIES
192b
194
RX DATA BUFFER(S)
106
SYSTEM BUS
DMA
TX_RING[3:0]_BASE
TX_RING[3:0]_LEN
TX_WR_PTR[3:0]
132
RX_RING[3:0]_BASE
RX_RING[3:0]_LEN
RX_WR_PTR[3:0]
STAT_RING[3:0]_BASE
STAT_RING[3:0]_LEN
RX_BUF_LEN
132
CURRENT CACHE LINE COPIES
132b
132a
STAT_WR_PTR COPIES
DESCRIPTOR MANAGEMENT SYSTEM
NETWORK CONTROLLER
130
102
108
NETWORK

Fig. 1E

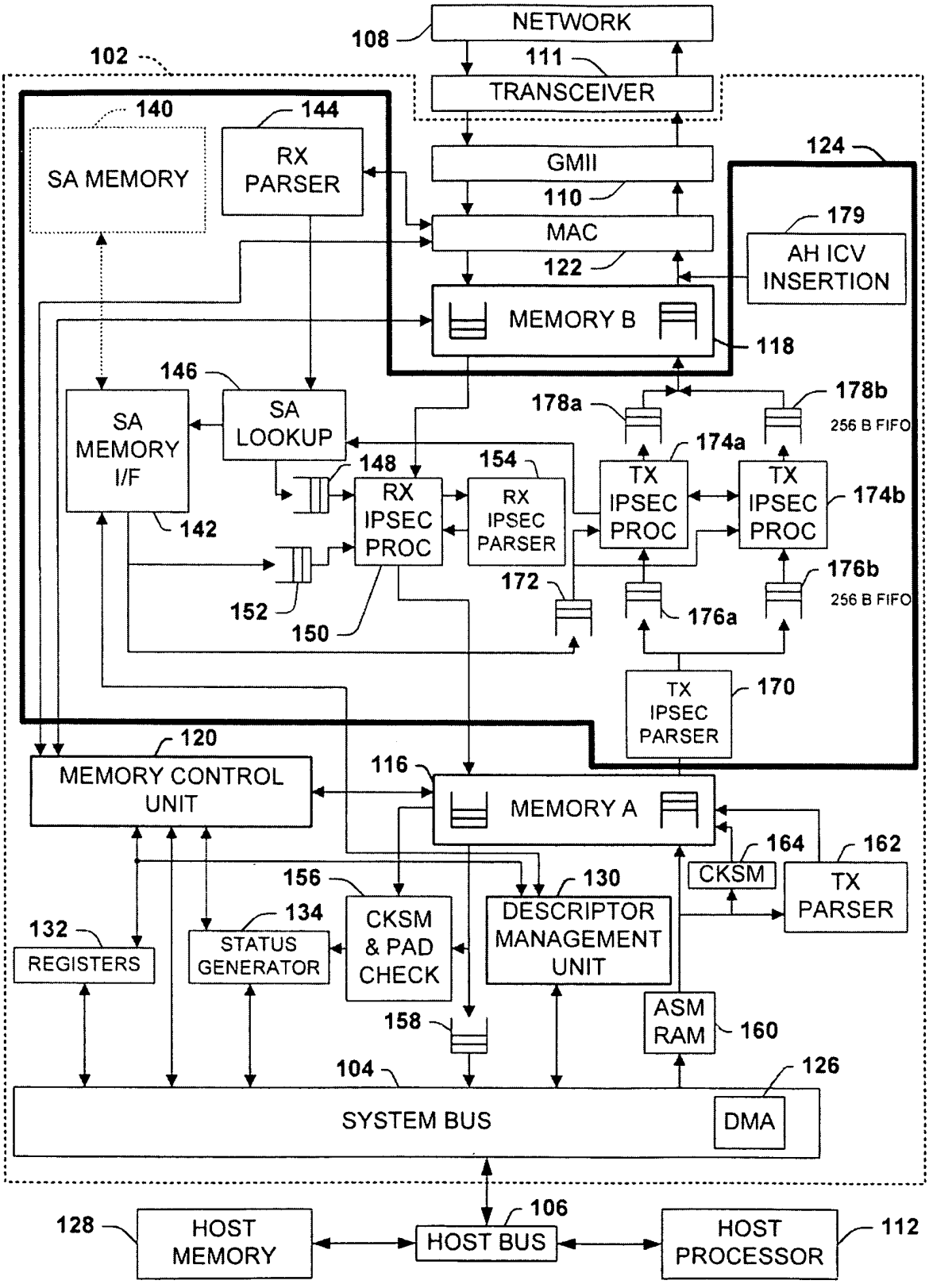
NETWORK
108
111
TRANSCEIVER
102
140
144
SA MEMORY
RX PARSER
GMII
124
110
179
MAC
AH ICV INSERTION
122
MEMORY B
118
146
SA LOOKUP
178a
178b
256 B FIFO
SA MEMORY I/F
174a
148
154
RX IPSEC PROC
RX IPSEC PARSER
TX IPSEC PROC
TX IPSEC PROC
174b
142
176b
256 B FIFO
172
152
150
176a
TX IPSEC PARSER
170
120
116
MEMORY CONTROL UNIT
MEMORY A
164
162
CKSM
TX PARSER
156
130
134
132
CKSM & PAD CHECK
DESCRIPTOR MANAGEMENT UNIT
STATUS GENERATOR
REGISTERS
ASM RAM
160
158
104
126
SYSTEM BUS
DMA
106
128
HOST MEMORY
HOST BUS
HOST PROCESSOR
112
180

Fig. 2

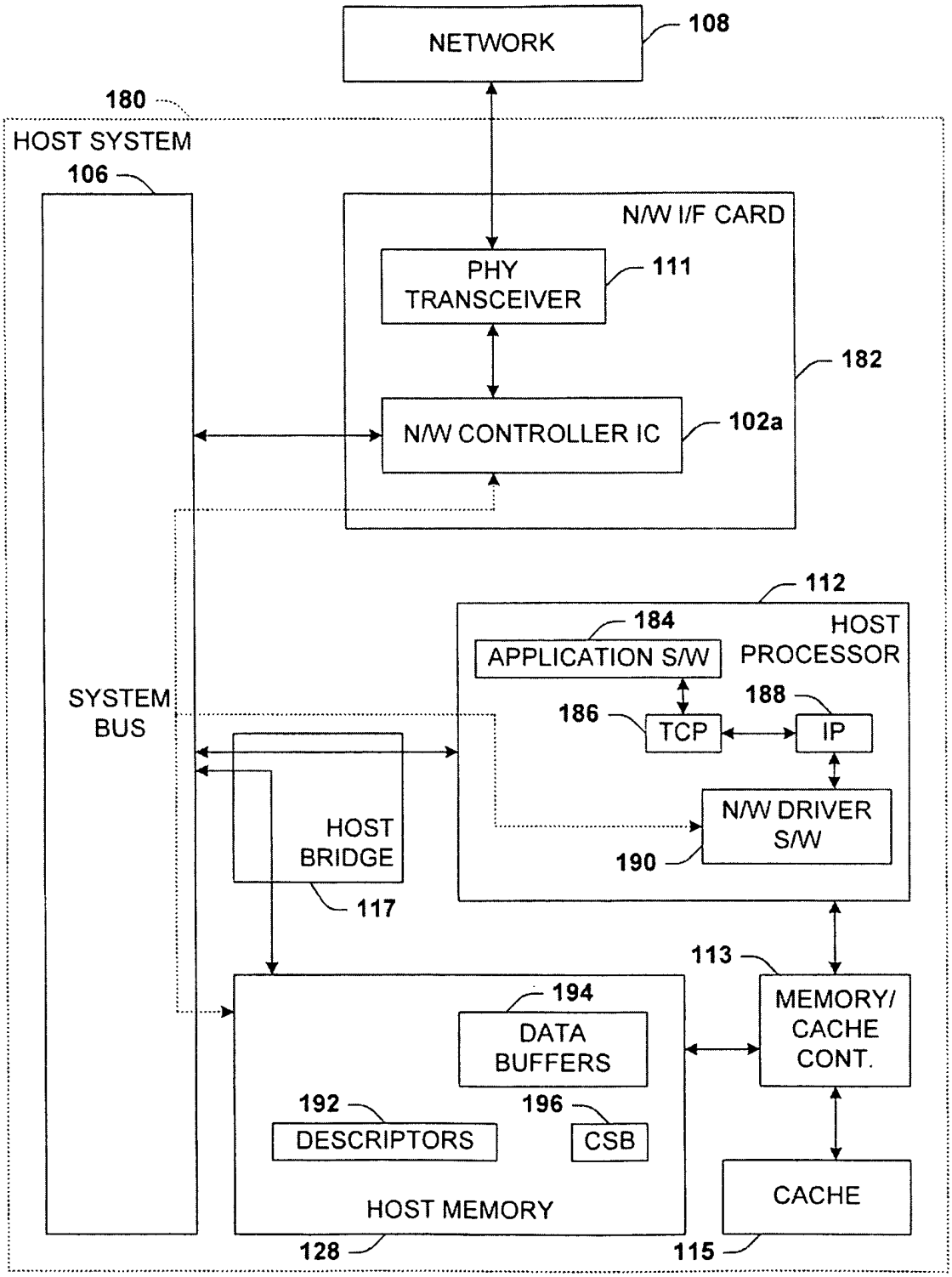
NETWORK
108
180
HOST SYSTEM
106
N/W I/F CARD
PHY TRANSCEIVER
111
182
N/W CONTROLLER IC
102a
112
HOST PROCESSOR
184
APPLICATION S/W
188
186
TCP
IP
N/W DRIVER S/W
190
SYSTEM BUS
HOST BRIDGE
117
113
MEMORY/ CACHE CONT.
194
DATA BUFFERS
192
DESCRIPTORS
196
CSB
HOST MEMORY
CACHE
128
115

Fig. 4

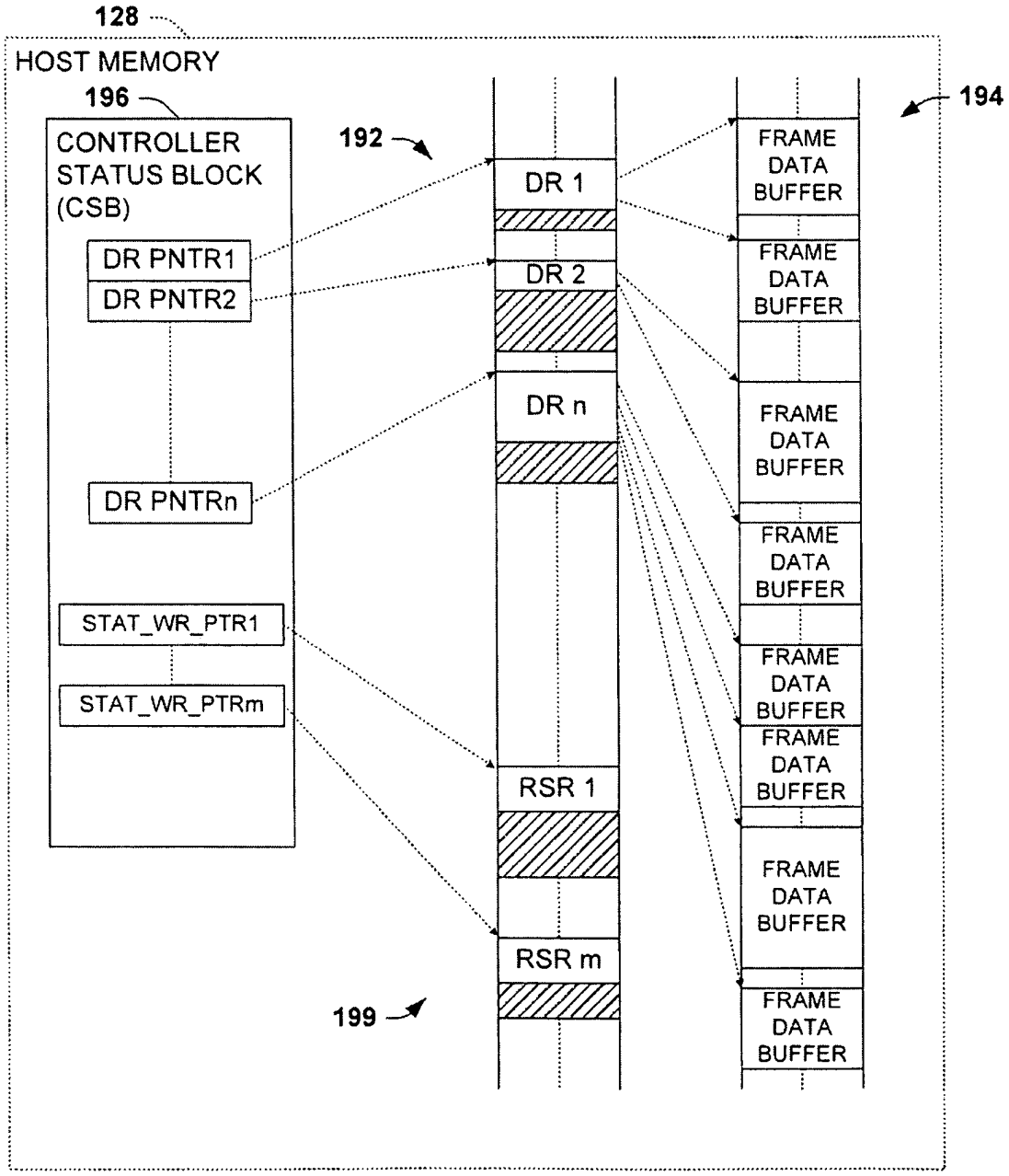
128
HOST MEMORY
196
CONTROLLER STATUS BLOCK (CSB)
DR PNTR1
DR PNTR2
DR PNTRn
STAT_WR_PTR1
STAT_WR_PTRm
192
DR 1
DR 2
DR n
RSR 1
RSR m
199
194
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER

Fig. 5A

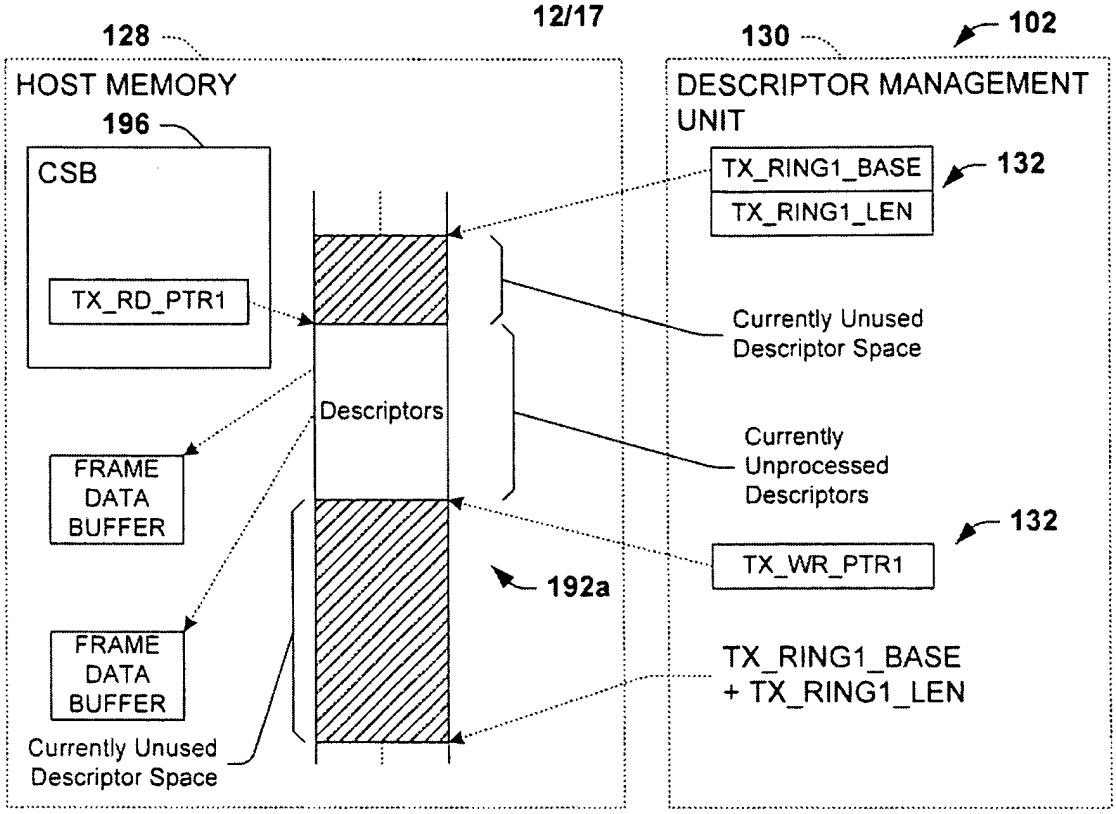

Fig. 5D

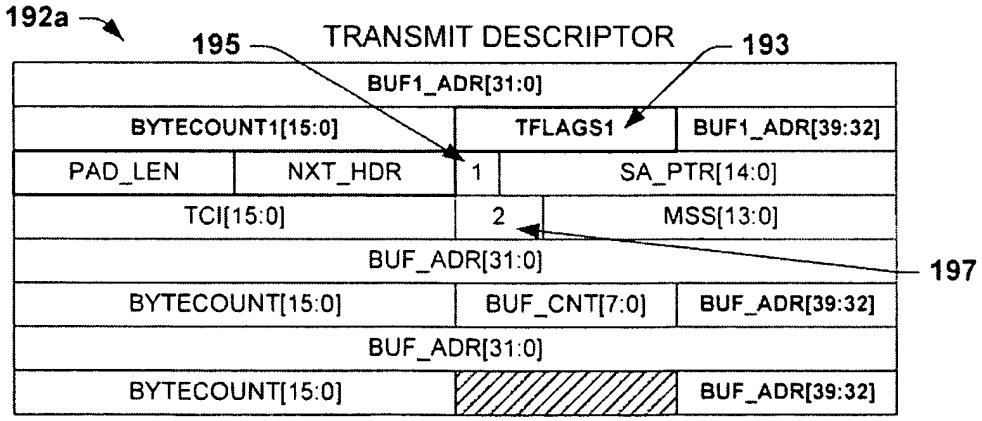

Fig. 5E

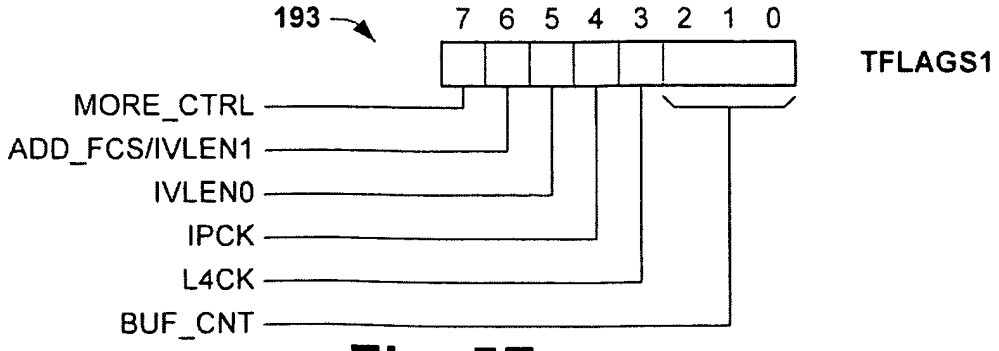

Fig. 5F

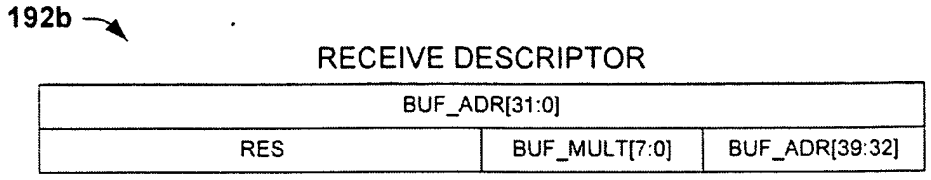
192b
RECEIVE DESCRIPTOR
BUF_ADR[31:0]
RES
BUF_MULT[7:0]
BUF_ADR[39:32]

Fig. 5G

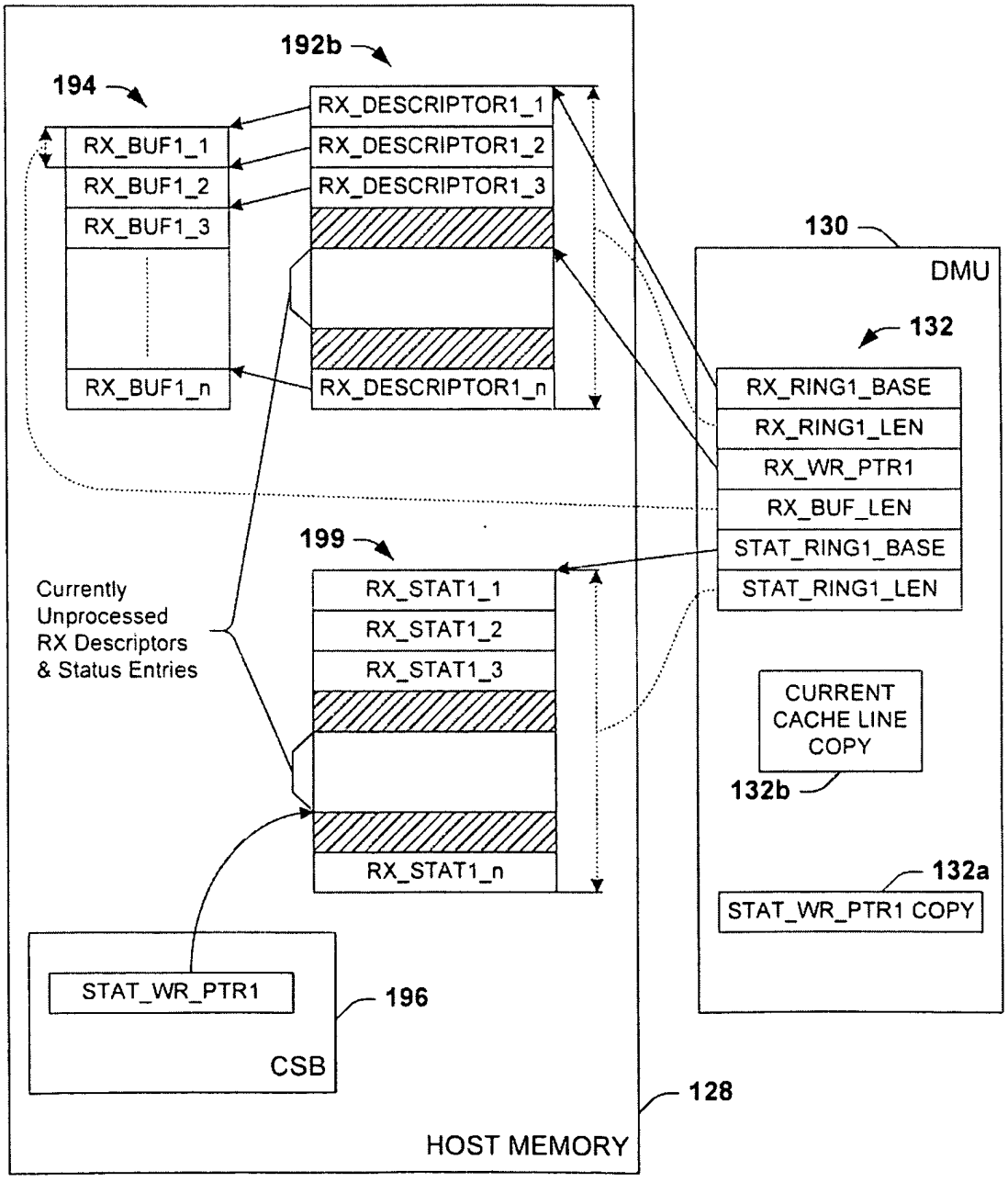
192b
194
RX_DESCRIPTOR1_1
RX_DESCRIPTOR1_2
RX_DESCRIPTOR1_3
RX_BUF1_1
RX_BUF1_2
RX_BUF1_3
RX_BUF1_n
RX_DESCRIPTOR1_n
130
DMU
132
RX_RING1_BASE
RX_RING1_LEN
RX_WR_PTR1
RX_BUF_LEN
STAT_RING1_BASE
STAT_RING1_LEN
199
Currently
Unprocessed
RX Descriptors
& Status Entries
RX_STAT1_1
RX_STAT1_2
RX_STAT1_3
RX_STAT1_n
CURRENT
CACHE LINE
COPY
132b
132a
STAT_WR_PTR1 COPY
STAT_WR_PTR1
196
CSB
128
HOST MEMORY

Fig. 5H

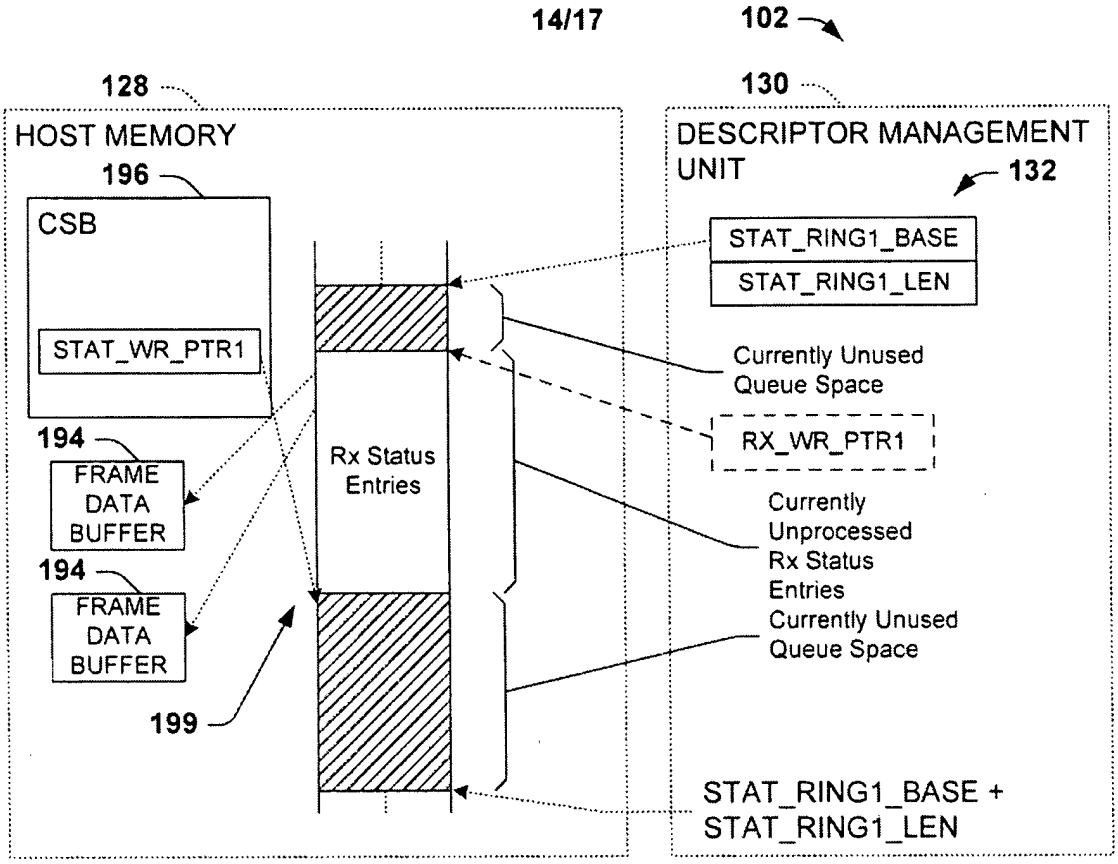
102
128
130
HOST MEMORY
196
CSB
STAT_WR_PTR1
194
FRAME DATA BUFFER
194
FRAME DATA BUFFER
199
Rx Status Entries
DESCRIPTOR MANAGEMENT UNIT
132
STAT_RING1_BASE
STAT_RING1_LEN
Currently Unused Queue Space
RX_WR_PTR1
Currently Unprocessed Rx Status Entries
Currently Unused Queue Space
STAT_RING1_BASE + STAT_RING1_LEN

Fig. 5I

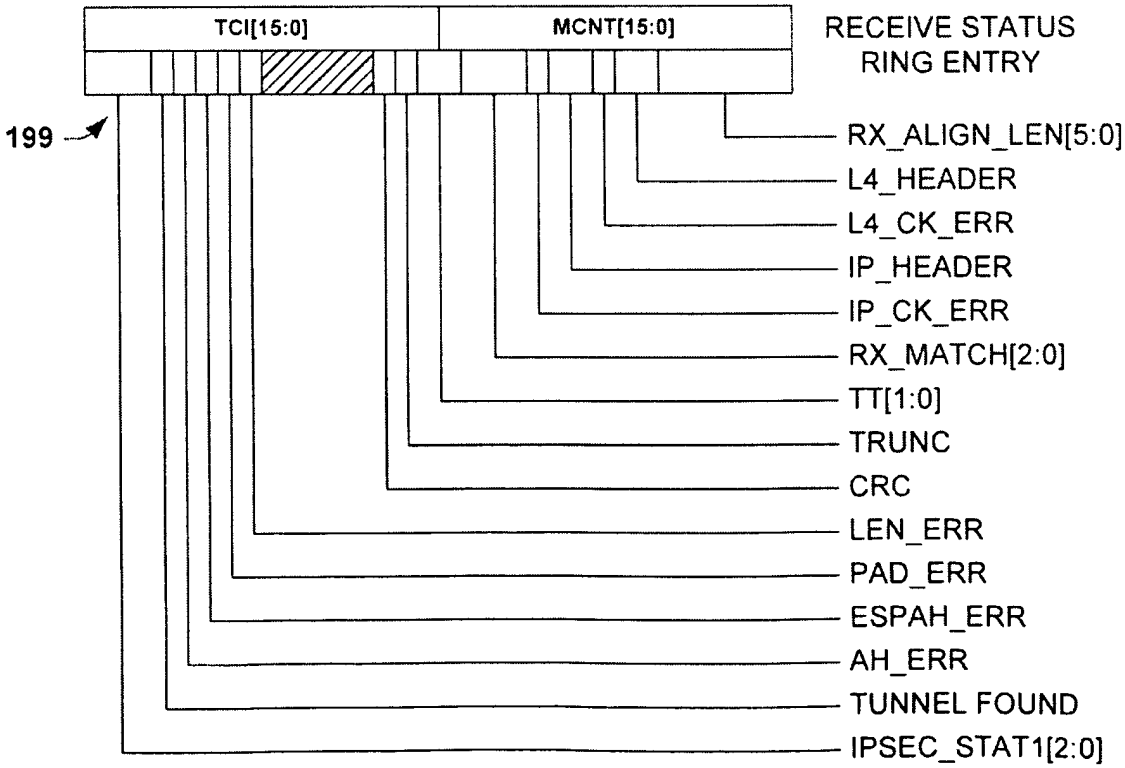
TCI[15:0]
MCNT[15:0]
RECEIVE STATUS RING ENTRY
199
RX_ALIGN_LEN[5:0]
L4_HEADER
L4_CK_ERR
IP_HEADER
IP_CK_ERR
RX_MATCH[2:0]
TT[1:0]
TRUNC
CRC
LEN_ERR
PAD_ERR
ESPAH_ERR
AH_ERR
TUNNEL FOUND
IPSEC_STAT1[2:0]

Fig. 5J

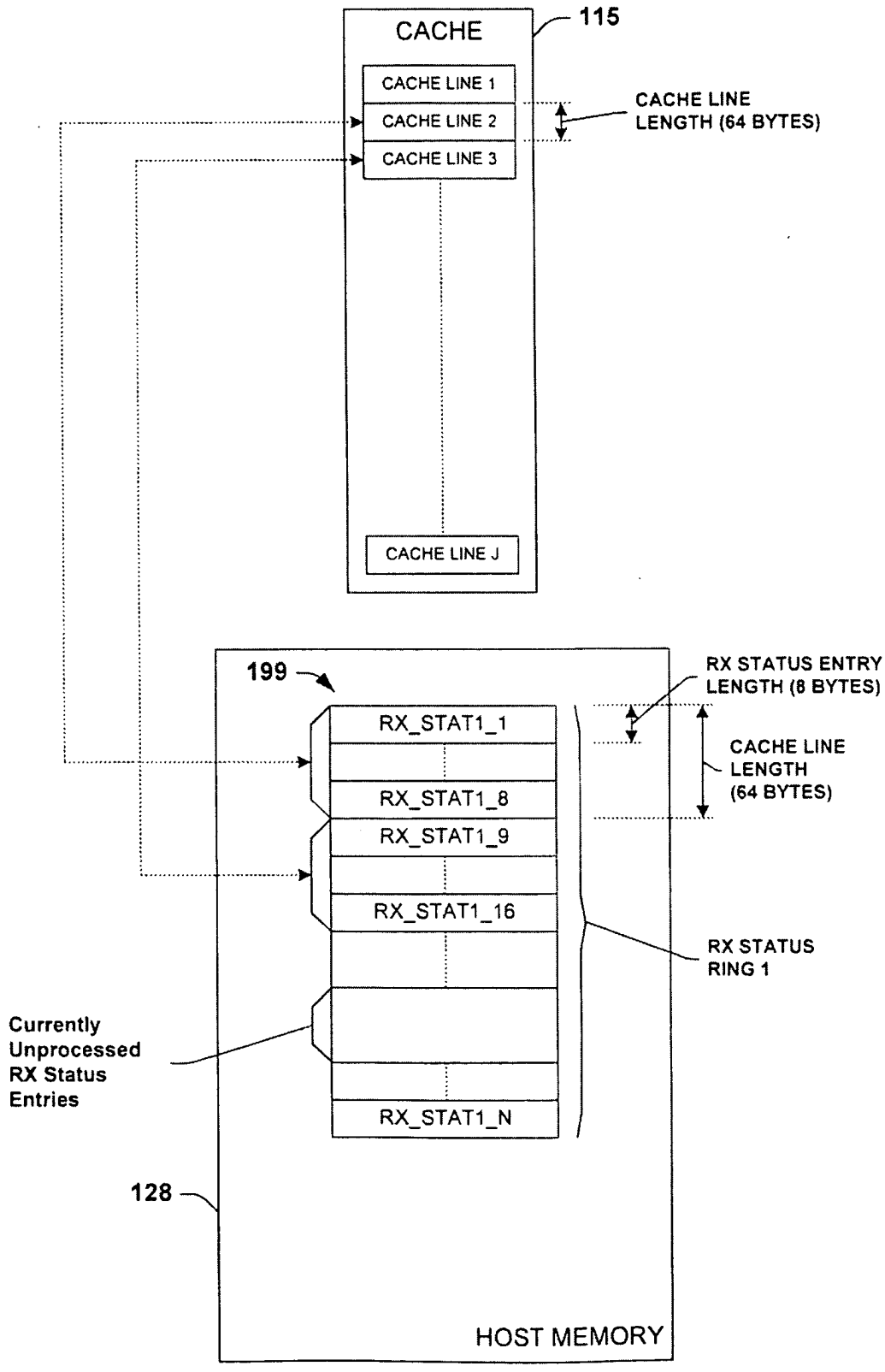
CACHE
115
CACHE LINE 1
CACHE LINE 2
CACHE LINE 3
CACHE LINE J
CACHE LINE LENGTH (64 BYTES)
199
RX STATUS ENTRY LENGTH (8 BYTES)
CACHE LINE LENGTH (64 BYTES)
RX_STAT1_1
RX_STAT1_8
RX_STAT1_9
RX_STAT1_16
RX_STAT1_N
RX STATUS RING 1
Currently Unprocessed RX Status Entries
128
HOST MEMORY

Fig. 6